SE4 Emerging & Disruptive Memory Technologies

Organizer / Chair: Sreedhar Natarajan, Emerging Memory Technologies, Kanata, Canada

This special session is organized to give the audience an outline of some of the emerging and disruptive memory technologies. Semiconductor Memories have been quite important forever and SRAMs, DRAMs and Flash have been the dominant ones for a long time. With technology scaling and current process and design complications, there is a need of new memory technologies that can be scalable and less expensive? Will process improve, quantify the problems and solve the current issues? Many of these questions have been addressed repeatedly and each time, when any of these questions are asked, a new memory technology surfaces.

SOI looks like a viable alternative now (been around for a long time) and the cost justified but the industry needs to prepare for this new material. The rapid changes in materials and process techniques leads to believe that the crossover between bulk and SOI may occur around 25nm. One of the talks will be on the SOI Twin Cell based memory which has immense advantages over their competition with improved performance and power.

The Thyristor Random Access memory, is an new emerging memory technology that is gaining rapid momentum in the industry and major advancements have been made in the cell manufacturability and drawing lot of market potential. The market and brief technical outline of TRAMs will be presented as well.

There is considerable driving force to create scalable elements and most of these new technologies lack scalability or are difficult to integrate due to complex process steps. To overcome these issues, a highly scalable resistance change memory using solid electrolytes will be discussed in detail.

NAND Flash seems to very competitive in the portable market and will this continue in future and how will it compete with larger mainstream HDD's? For the storage market, which technology is going to cover the terabit storage, the next talk will outline the technologies required to take the industry to the Terabit storage capacity.

Position Statements

SOI TwinCell RAM Technology

Kazutami Arimoto, Renesas, Osaka, Japan

SOI device is currently used in limited applications and not adequate wafers are not produced in volume yet. However from the view point of device technologies, SOI technologies will become mainstream for SOC solutions at 45nm and below. Especially, the combination of circuit techniques with the SOI unique device structure enhances several merits to overcome the device limitations in bulk. Memory occupation ratio in SoC is increasing and SRAM bit cell size has been shrinking with technology scaling and new high density memories are being proposed to compete in that market. However, even if the new memory technologies are developed, system integration strongly requires "CMOS compatible technologies". So the key definitions of future memories for SoC with SOI devices are "High density, low power, and CMOS compatibility". This breakthrough SOI Twincell technology will discuss the practical SoC memory solutions beyond 45nm era.

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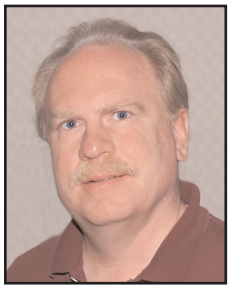

Thyristor RAM: Evolving and Disruptive Memory Technology

Bruce Bateman, T-RAM Inc, San Jose, CA

T-RAM memory technology represents the first production worthy “new” high performance Random Access Memory technology to be introduced in decades. The TRAM memory cell is 1/4 the size of 6-T SRAM on the same technology node and offers RAM array sizes 1/2 to 1/3 the size of 6-T SRAM based arrays at the same random-access read performance and similar or lower power. The technology is easily and inexpensively retrofitted to existing CMOS processes and is scalable with improving device characteristics to 45nm and below.

Small Hard Disk Drives vs. Solid State Storage

Barry Stipe, Hitachi, San Jose, CA

Today NAND flash and small Hard Disk Drives (HDDs) compete directly for use in portable devices such as music players, digital cameras and video players, and soon even in converged devices such as high-end cell phones. How will this battle play out in the future? Will ultra-small HDDs such as HitachiGST's "Mikey" drive maintain its capacity advantage over flash storage in the future? Can a future solid state technology ever compete with larger mainstream HDDs? In this talk I review the HDD technologies necessary to achieve greater than a Terabit of memory capacity in a sub-CF form factor. These technologies include perpendicular recording, tilted recording, thermally-assisted recording, and patterned media. Comparisons between the flash roadmaps and HDD roadmaps will be made.

Highly Scalable Resistance-Change Memory Using Solid Electrolytes

Michael N. Kozicki, Axon Technologies Corporation & Arizona State University, AZ

There is a considerable driving force within the semiconductor industry to create scalable elements that can switch between widely spaced non-volatile resistance states at very low power. Such elements could find widespread application in next generation memory and logic. Whereas there are several new technologies that show promise in this respect, they typically lack complete scalability, i.e., they have a physical size, programming voltage, or programming current that is excessive for high density integrated systems beyond the 45 nm node of the ITRS Roadmap. Many are also difficult to integrate due to the complexities associated with the additional processing steps and masking levels required and therefore will be expensive to add to highly-scaled CMOS. One potential approach to this problem involves switching elements which utilize the reduction of nanoscale quantities of metal ions in solid electrolyte films. A silver- or copper-containing layer and an inert electrode formed in contact with a Ag or Cu ion-containing electrolyte film creates a device in which information is stored via electrical changes caused by the oxidation of the metal electrode and reduction of the mobile metal ions in the electrolyte. Resistance reduction of many orders of magnitude is attainable within a few tens of nanoseconds or less for voltages of a few hundred mV and currents in the μA range. A similarly small opposite bias reverses the process to erase the device. In addition to possessing the endurance, retention, and CMOS compatibility required of future memory, such devices have excellent scaling prospects due to their low operational power and physical scalability to the sub-10 nm regime. This talk will review the state-of-the-art in devices based on solid electrolytes and will discuss technology and design aspects for ultra high density memory and storage.